PENDING CLAIMS

Current listing of the claims:

1. (Original) In a communication system, a method comprising:

encoding a block of data at an encoding rate 1/R, wherein said encoding produces R number of data symbols for every data bit in said block of data, thereby producing R blocks of data;

partitioning a block of RAM into a plurality of blocks of RAM;

writing data symbols of said R blocks of data into said plurality of blocks of RAM, wherein said writing is according to a predefined interleaving function.

2. (Original) The method as recited in claim 1 further comprising:

sequentially reading data symbols from each block of said plurality of blocks of RAM.

3. (Original) The method as recited in claim 2 wherein said sequential reading begins at a first RAM block of said plurality of blocks of RAM.

4. (Original) The method as recited in claim 3 wherein said sequential reading continues to a second RAM block of said plurality of blocks of RAM.

5. (Original) The method as recited in claim 4 wherein said sequential reading ends at said second RAM block of said plurality of blocks of RAM.6. The method as recited in claim 4 wherein said sequential reading continues to a third RAM block of said plurality of blocks of RAM.

7. (Original) The method as recited in claim 6 wherein said sequential reading ends at said third RAM block of said plurality of blocks of RAM.

8. (Original) The method as recited in claim 2 wherein said block of data is associated with a first frame of data, thereby said writing is associated with said first frame of data, wherein said reading is associated with a second frame of data, said second frame of data being in advance of said first frame of data for transmission from said communication system, and wherein said reading and writing are taking place simultaneously in respectively two sets of said plurality of blocks of RAM, wherein one set is associated with said writing and another set with said reading.

9. (Original) The method as recited in claim 1 further comprising partitioning each block of said plurality of blocks of RAM to at least two sub-blocks of RAM.

10. (Original) The method as recited in claim 9 wherein, via said writing step, one of said least two sub-blocks of RAM stores in-phase data symbols, and another quad-phase data symbols.

11. (Original) The method as recited in claim 10 further comprising:

sequentially reading data symbols from each block of RAM of said plurality of blocks of RAM, wherein said reading includes reading said least two RAM sub-blocks simultaneously, thereby producing, simultaneously, an in-phase data symbol and a quad-phase data symbol.

12. (Original) The method as recited in claim 11 further comprising:

scrambling said in-phase data symbols to produce scrambled in-phase data symbols.

13. (Original) The method as recited in claim 11 further comprising:

scrambling said quad-phase data symbols to produce scrambled quad-phase data symbols.

14. (Original) The method as recited in claim 11 further comprising:

scrambling simultaneously said in-phase data symbols and quad-phase data symbols to produce scrambled in-phase data symbols and quad-phase data symbols.

15. (Original) The method as recited in claim 14 further comprising:
Walsh covering said scrambled in-phase and quad-phase data bits to produce Walsh covered in-phase and quad-phase data bits, wherein said Walsh covering is according to a Walsh code assigned to a communication channel in said communication system.

16. (Original) The method as recited in claim 15 further comprising:

summing said Walsh covered in-phase and quad-phase data symbols with respectively other Walsh covered in-phase and quad-phase data symbols to produce a summed Walsh covered in-phase and quad-phase data symbols.

17. (Original) The method as recited in claim 16 further comprising:
spreading said summed Walsh covered in-phase and quad-phase data symbols according to one of a QPSK and BPSK spreading schemes to produce a spread spectrum signal for transmission from said communication system.

18. (Original) A communication system comprising:

a channel encoder for encoding channel data;
a block interleaver for interleaving encoded data symbols produced by said channel encoder to produce simultaneously in-phase interleaved data symbols and quad-phase interleaved data symbols.

19. (Original) The communication system of claim 18 further comprising:

a long code generator having an I-output and a Q-output for scrambling respectively said in-phase and quad-phase data symbols;
an I-scrambler and a Q-scrambler for scrambling simultaneously, using said I and Q outputs, respectively said in-phase and quad-phase data symbols to produce simultaneously scrambled in-phase and quad-phase data symbols.

20. (Original) The communication system of claim 19 further comprising:

a QPSK/BPSK spreader receiving said scrambled in-phase and quad-phase data symbols to produce a spread spectrum signal for transmission from said communication system.

21. (Original) The communication system of claim 20 further comprising:

a Walsh code covering block for Walsh covering said scrambled in-phase and quad-phase data symbols before said QPSK/BPSK spreader for producing said spread spectrum signal for transmission from said communication system.